WE CLAIM:

1. A high-performance, high I/O ball grid array substrate, designed for integrated circuit flip-chip assembly and having two patterned metal layers, comprising:

an insulating layer having a first surface, a second surface and a plurality of vias filled with metal;

said first surface having one of said metal layers attached to provide electrical ground potential, and having a plurality of electrically insulated openings for outside electrical contacts;

an outermost insulating film protecting the exposed surface of said ground layer, said film having a plurality of openings filled with metal suitable for solder ball attachment;

said second surface having the other of said metal layers attached, portions thereof being configured as a plurality of electrical signal lines, further portions as a plurality of first electrical power lines, and further portions as a plurality of second electrical power lines, selected signal and power lines being in contact with said vias;

said signal lines being distributed relative to said first power lines such that the inductive coupling between them reaches at least a minimum value, providing high mutual inductances and minimized effective self-inductance;

said signal lines further being electromagnetically coupled to said ground metal such that cross-talk between signal lines is minimized; and

an outermost insulating film protecting the exposed surfaces of said signal and power lines, said film having a plurality of openings filled with metal suitable for contacting selected signal and power lines and chip solder bumps.

2. The substrate according to Claim 1 wherein the number of said I/O's ranges from about 100 to about 600.

3. The substrate according to Claim 1 wherein the thickness of said substrate is in the range from about 150 to 300 μm.

4. The substrate according to Claim 1 wherein said signal lines have a width between about 25 to 60 μm and are spaced to an adjacent line by insulating material of about 20 to 50 μm width.

5. The substrate according to Claim 1 wherein said first power lines have a width from about 200 to 500 μm.

6. The substrate according to Claim 1 wherein said signal lines are positioned in a proximity of about 20 to 50 μm to said first power lines, thus providing strong electromagnetic coupling, high mutual inductance and minimized effective self-inductance.

7. The substrate according to Claim 1 wherein said signal lines are positioned to provide strong electromagnetic coupling to power and ground lines and thus minimal coupling, or cross-talk, between said signal lines.

8. The substrate according to Claim 1 wherein said patterned metal layers are selected from a group consisting of copper, brass, aluminum, silver, or alloys thereof, and have a thickness in the range from about 7 to 15 μm.

9. The substrate according to Claim 1 wherein said insulating layer is made of organic material and is

selected from a group consisting of polyimide, polymer strengthened by glass fibers, FR-4, FR-5, and BT resin; said insulating layer having a thickness between about 70 and 150 μm.

10. The substrate according to Claim 1 wherein said vias are filled with copper, tungsten, or any other electrically conductive material.

11. The substrate according to Claim 1 wherein said second power lines are structured as distributed areas having wide geometries for minimizing self-inductance and merging into a central area supporting said chip.

12. The substrate according to Claim 1 wherein said outermost insulating films are glass-filled epoxies, polyimides, acrylics or other photo-imageable materials suitable as solder masks and have a thickness between about 50 and 100 μm.

13. The substrate according to Claim 1 wherein said openings for solder bump and solder ball attachments are made of copper including a flash of gold or palladium, or other wettable and solderable metals.

14. A high-performance, high I/O ball grid array package comprising:

a substrate having two patterned metal layers, comprising:

an insulating layer having a first surface, a second surface and a plurality of vias filled with metal;

said first surface having one of said metal layers attached to provide electrical ground potential, and having a plurality of electrically insulated openings for outside electrical contacts;

an outermost insulating film protecting the exposed surface of said ground layer, said film having a plurality of openings filled with metal suitable for solder ball attachment;

said second surface having the other of said metal layers attached, portions thereof being configured as a plurality of electrical signal lines, further portions as a plurality of first electrical power lines, and further portions as a plurality of second electrical power lines, selected signal and power lines being in contact with said vias;

said signal lines being distributed relative to said first power lines such that the inductive coupling between them reaches at least a minimum value, providing high mutual inductances and minimized effective self-inductance;

said signal lines further being electromagnetically coupled to said ground metal such that cross-talk between signal lines is minimized; and

an outermost insulating film protecting the exposed surfaces of said signal and power lines, said film having a plurality of openings filled with metal suitable for contacting selected signal and ground lines and chip solder bumps;

an integrated circuit chip having an active surface including solder bumps, said solder bumps adhered to said plurality of openings in said outermost

insulating film protecting said signal and power lines; and

solder balls attached to said plurality of openings in said outermost insulating film protecting said ground layer.

15. The package according to Claim 14 further comprising a polymeric encapsulant filling any gaps between said chip and said substrate, left void after said chip solder bumps are adhered to said plurality of openings in said outermost insulating film protecting said signal and power lines.

16. The package according to Claim 15 wherein said polymeric encapsulant is a polymeric precursor made of an epoxy base material filled with silica and anhydrides, requiring thermal energy for curing to form a polymeric encapsulant.

17. The package according to Claim 14 further comprising an encapsulation material surrounding said chip.

18. The package according to Claim 17 wherein said encapsulation material is a polymeric material selected from a group consisting of epoxy-based molding compounds suitable for adhesion to said chip, and fluoro-dielectric compounds supporting high-speed and high-frequency package performance.

19. The package according to Claim 17 further comprising an optional heat spreader positioned on the outer surface of said encapsulation material.

20. The package according to Claim 14 wherein said chip solder bumps comprise attach materials selected from a group consisting of tin, lead/tin alloys, indium, indium/tin alloys, solder paste, and conductive adhesive compounds.

21. The package according to Claim 14 wherein said solder balls comprise attach materials selected from a group consisting of tin/lead, tin/indium, tin/silver, tin/bismuth, solder paste, and conductive adhesive compounds.

22. The package according to Claim 14 wherein the thickness of said package is in the range from about 250 to 800 μm, excluding the thickness of the heat slug.

23. A computer-implemented method for modeling a high-performance, high I/O ball grid array substrate, intended for integrated circuit flip-chip assembly and having a first and a second metal layer and one intermediate insulating layer, all of substantially equal areas, comprising the steps of:

modeling the structure of said first metal layer as electrical ground potential, said layer having a plurality of electrically insulated openings for electrical contacts;

modeling the structure of said second metal layer as a plurality of electrical signal lines, a plurality of first electrical power lines operable at a first potential, and a plurality of second electrical power lines operable at a second potential;

configuring said first power lines so wide that their combined inductances approximate the inductance of a metal having the size of the total substrate;

concurrently distributing said first power lines among said signal lines in order to provide at least minimum inductive coupling between signal and power lines, thereby obtaining high mutual

inductances and minimizing effective self-inductance;

configuring said second power lines to serve as distributed areas having wide geometries for minimizing self-inductance and merging into a central area supporting said chip; and

modeling the structure of said insulating layer for positioning it between said first and second metal layers, and selecting its thickness and material characteristics suitable for strong electromagnetical coupling between said signal lines and said first metal layer, thereby providing a predetermined impedance to ground and minimizing cross-talk between signal lines.

24. A method for fabricating a high performance, high I/O ball grid array substrate, intended for two patterned metal layers and integrated circuit flip-chip assembly, comprising the steps of:

providing an electrically insulating layer having a first and a second surface;

forming a plurality of via holes in said insulating layer and filling said holes with electrically conductive material;

attaching one of said metal layers to said first surface, said metal layer intended to provide electrical ground potential;

forming a plurality of electrically insulated openings in said metal layer, said openings intended for outside electrical contacts;

attaching the other of said metal layers to said second surface, said metal layer intended to provide electrical signal and power potentials;

configuring portions of said metal layer as a plurality of electrical signal lines, further portions as a plurality of first electrical power lines, and further portions as a plurality of second electrical power lines, thereby creating contact between selected signal and power lines and said vias;

forming an insulating protective film over the exposed surface of said ground layer, and an insulating film over the exposed surfaces of said signal and power lines; and

forming pluralities of openings in both said insulating films, and filling said openings with solderable metal, thereby creating attachment sites for outside solder balls and for chip solder bumps.

25. The method according to Claim 24 further comprising the step of attaching an integrated circuit chip, having an active surface including solder bumps, by adhering said solder bumps to said plurality of metal-filled openings in said outermost insulating film protecting said signal and power lines.

26. The method according to Claim 25 further comprising the step of filling with a polymeric encapsulant any gaps between said substrate and said chip left void after said chip solder bumps are adhered to said plurality of openings in said outermost insulating film protecting said signal and power lines.

27. The method according to Claim 24 further comprising the step of surrounding said chip with a polymeric encapsulation compound.

28. The method according to Claim 27 further comprising the

step of attaching a heat spreader positioned on the outer surface of said encapsulation material.

29. The method according to Claim 24 further comprising the step of attaching solder balls to said plurality of metal-filled openings in said outermost insulating film protecting said ground layer.